1. A latency compensation circuit for use in a first wireless access point operating in accordance with a communications protocol comprising:

a first acquisition circuit for identifying receipt of a first data packet from a second wireless access point;

a speculative response circuit for issuing a speculative response to said first data packet to said second wireless access point;

wherein said speculative response is transmitted by said first access point before said first wireless access point has completed a packet decoding operation on said first data packet.

2. The latency compensation circuit of claim 1, wherein said speculative response is a pre-stored preamble.

3. The latency compensation circuit of claim 1, wherein said packet decoding operation is associated with a multi-antenna signal processing circuit operating on N separate received data signals, where N>1.

4. The latency compensation circuit of claim 1, wherein said speculative response is generated to ensure that said first wireless access point complies with timing requirements of said communications protocol.

5. The latency compensation circuit of claim 4, wherein said timing requirements are associated with a Short Inter-Frame Spacing (SIFS) interval of an 802.11x compatible data link.

6. The latency compensation circuit of claim 5, wherein said SIFS interval is less than half a latency time associated with said packet decoding operation.

7. The latency compensation circuit of claim 1, wherein an acknowledgement transmission packet and a received packet are processed simultaneously.

8. The latency compensation circuit of claim 1, wherein said first wireless access point is configured in a contention free period (CFP) mode.

9. The latency compensation circuit of claim 8, wherein said first wireless access point determines an access sequence for a wireless medium with respect to other access points to identify said CFP.

10. An access radio frequency (RF) multi-antenna access point system comprising:

a multi-antenna signal processing circuit situated in a first access point and adapted to:

(a) receive M separate data packets from a second access point representing a single multiplexed data stream;

(b) process said M separate data packets during a packet decoding operation, which packet decoding operation requires a first time period;

(c) generate a packet acknowledgement when a data packet is received, and prior to an expiration of said first time period, so that a processing latency associated with said packet decoding operation does not cause a violation of a timing requirement in a wireless medium used by said first access point.

11. The circuit of claim 10, wherein said multi-antenna signal processing circuit is enabled and selectively transmits only when channel conditions indicate that a data rate in said channel has fallen below a predetermined threshold.

12. The circuit of claim 10, wherein said multi-antenna signal processing circuit is enabled and selectively transmits in response to a determination that a data rate in said channel is to be enhanced above a nominal operating rate.

13. The circuit of claim 10, wherein said multi-antenna signal processing circuit is enabled and selectively transmits in response to a determination that frequency selective fading is present in said channel.

14. The circuit of claim 10 wherein said multi-antenna signal processing circuit is situated in a signal path ahead of a first baseband processor, and is further adapted to monitor channel transmission conditions to identify whether an operation of said first baseband processor should be enhanced.

15. The circuit of claim 10, wherein said timing requirement is associated with an 802.11x communications protocol.

16. The circuit of claim 10 wherein said packet acknowledgement is a dummy data value for a transmission packet preamble.

17. The circuit of claim 10 wherein said multi-antenna signal processing circuit is configured as a multiple-in, multiple out (MIMO) processor.

18. The circuit of claim 10, wherein said multi-antenna signal processing circuit demodulates a data stream transmitted using multiple independent antennas which each transmit a portion of said data stream.

19. A radio frequency (RF) multi-antenna access point system implemented in a single chip integrated circuit chip (IC) comprising:

a baseband processor circuit located in a first portion of the single chip IC for handling data transmissions during a first operating mode in a channel between a first access point and a second access point;

a multi-antenna signal processing circuit located in a second portion of the single chip IC for handling data transmissions during a second operating mode in said channel, said multi-antenna signal processing circuit being further adapted to:

(a) receive M independent RF modulated input signals from said second access point;

(b) process said M independent RF modulated input signals using a channel mixing matrix to extract N independent data signals transmitted by said second access point;

wherein said first operating mode and said second operating mode are automatically selected by the RF multi-antenna access point system based on a transmission condition in said channel;

(c) generate a transmission acknowledgement when said M independent RF modulated data signals are received, and prior to an expiration of step (b) so that a processing latency of said multi-antenna signal processing circuit does not cause a violation of a timing requirement in a wireless medium used by said first access point.

20. The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit includes an analog to digital converter, and a digital to analog converter for interfacing to an antenna.

21. The RF multi-antenna access point system of claim 20, wherein said multi-antenna signal processing circuit includes a Fast Fourier Transform (FFT) Circuit.

22. The RF multi-antenna access point system of claim 21, wherein said multi-antenna signal processing circuit includes a preamble acquisition circuit for performing a preamble acquisition to align an FFT data frame with an 802.11x based data stream.

23. The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit processes at least 4 separate input signals representing a data stream multiplexed over 4 separate bit streams.

24. The RF multi-antenna access point system of claim 19, wherein said channel mixing matrix performs an operation that computes a recovered data signal x as follows:

$$x = b1*y1 + b2*y2 + x0$$

where b1 and b2 are equalization coefficients computed by said multi-antenna signal processing circuit, y1 and y2 are received data from separate baseband channels, and x0 is a recovered signal from an adjacent channel.

25. The RF multi-antenna access point system of claim 19, wherein space division multiple access is realized by separating different RF signals from different signal paths simultaneously in the single chip IC.

26. The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit extends a data transmission range achieved by said baseband processor circuit between said first access point and said second access point.

27. The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit increases a data transmission rate achieved by said baseband processor circuit between said first access point and said second access point.

28. The RF multi-antenna access point system of claim 19, wherein said multi-antenna signal processing circuit transmits M separate data signals to said second access point.

29. The RF multi-antenna access point system of claim 28, wherein a localized encryption is achieved for said second access point by independently controlling said M separate transmission signals.

30. The circuit of claim 19, wherein said timing requirement is associated with an 802.11x communications protocol.